

**EAST - [10691173.wsp:1]**

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memory and vertical near transistor\$1 and trench near capacitor\$1

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	U	I	Document ID	Issue Date	Pages	Title	Current OR	Current XRef	
222	<input checked="" type="checkbox"/>	<input type="checkbox"/>	US 6756622 B2	20040629	21	Vertical gain cell and array for a dynamic random access memory and method for forming the same	257/296	257/301; 257/E27.064	
223	<input checked="" type="checkbox"/>	<input type="checkbox"/>	US 6750098 B2	20040615	12	Integrated semiconductor memory and fabrication method	438/244	257/302; 257/307; 257/E21.652	
224	<input checked="" type="checkbox"/>	<input type="checkbox"/>	US 6747306 B1	20040608	9	Vertical gate conductor with buried contact layer for increased contact landing area	257/302	257/301	
225	<input checked="" type="checkbox"/>	<input type="checkbox"/>	US 6747305 B2	20040608	22	Memory address decode array with vertical transistors	257/302	257/296; 257/908	
226	<input checked="" type="checkbox"/>	<input type="checkbox"/>	US 6741519 B2	20040525	14	DRAM technology compatible processor/memory chips	365/230.06	326/105; 326/106; 365/149	
227	<input checked="" type="checkbox"/>	<input type="checkbox"/>	US 6740920 B2	20040525	8	Vertical MOSFET with horizontally graded channel doping	257/302	257/328; 257/329	
228	<input checked="" type="checkbox"/>	<input type="checkbox"/>	US 6740917 B2	20040525	8	Integrated semiconductor memory fabrication method	257/296		
229	<input checked="" type="checkbox"/>	<input type="checkbox"/>	US 6737316 B2	20040518	20	Method of forming a deep trench DRAM cell	438/244	257/E21.652; 257/E21.653; 257/E21.703	
230	<input type="checkbox"/>	<input type="checkbox"/>	US 6734485 B2	20040511	36	Vertical DRAM cell structure and its contactless DRAM arrays	257/301	257/302	
231	<input checked="" type="checkbox"/>	<input type="checkbox"/>	US 6734484 B2	20040511	32	Vertical transistor DRAM structure and its manufacturing methods	257/301	257/302; 257/304; 257/305	
232	<input checked="" type="checkbox"/>	<input type="checkbox"/>	US 6727539 B2	20040427	17	Embedded vertical DRAM arrays with slidded bitline and polysicon interconnect	257/296	257/288; 257/E21.659; 257/E21.66	